US-PAT-NO: 5943564

DOCUMENT-IDENTIFIER: US 5943564 A

TITLE: BiCMOS process for forming double-poly MOS and bipolar transistors with substantially identical device architectures

---------- KWIC ---------

Optionally, rather than implanting the n+ and p+ materials through the layer of oxide 132, the n+ and p+ materials can be implanted through a temporary layer of screen oxide . With this option, a layer of screen oxide approximately 150 .ANG. thick is first formed over the layer of poly-1 130. Following this, the n+/p+ masking and implanting steps are performed as described above. Once the

n+/p+ materials have been implanted, the layer of screen oxide is removed, followed by the deposition of the layer of oxide 132.

US-PAT-NO: 5976956

DOCUMENT-IDENTIFIER: US 5976956 A

TITLE: Method of controlling dopant concentrations using transient-enhanced diffusion prior to gate formation in a device

---------- KWIC ---------

Several techniques are alternatively performed to form shallow source/drain junctions for submicron CMOS devices. In one example, arsenic is implanted for N-channel devices and BF.sub.2.sup.+ is implanted for P-channel devices since both species have shallow ranges at typical implant energies of 30 keV to 50 keV implanted through a screen oxide to protect source-drain regions from implant contamination. The silicon substrate 102 is preamorphized by implanting silicon (Si) or germanium (Ge) to reduce channeling and produce shallow junctions. The implanted species is diffused past the layer of implant damage that is not annealed out to prevent junction leakage. Rapid thermal anneal techniques are used to perform the anneal and diffusion thermal cycles. Shallow p.sup.+ n junctions formed using diffusion is also used. The screen oxide is damaged and often contaminated following the source-drain implant and is therefore stripped following the source-drain implant. Another oxide layer is grown over the source-drain regions and on the sidewall of the etched

US-PAT-NO: 6352936

DOCUMENT-IDENTIFIER: US 6352936 B1

TITLE: Method for stripping ion implanted photoresist layer

---------- KWIC ---------

Ion implantation is performed through a screen oxide . This is a sacrificial oxide that is used to reduce channelling. The thickness of this screen oxide ranges from 15 to 40 nm. When scaling down devices, two implantation steps are performed subsequently to form source and drain regions, using the same screen oxide of typically 15 nm and two different photoresist masks. To be able to do this, oxide loss during stripping, especially for the first photoresist layer, must be minimised.

Implantation of phosphorus was performed through a 15 nm screen oxide, using a
medium current ion implanter from Eaton. Implantation (I) and RIE strip (S) parameters are mentioned in table 1.

Fig.1(a)

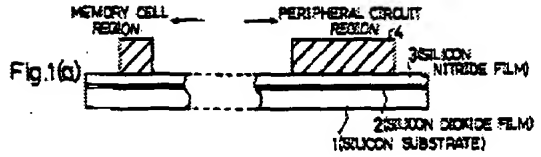


Fig.1(b)

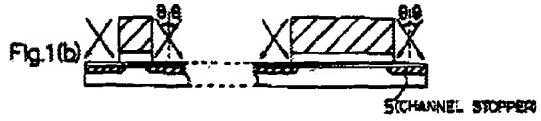


Fig.1(c)

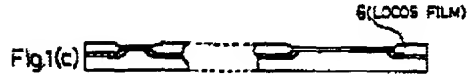
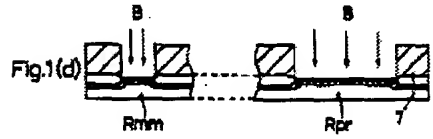


Fig.1(d)



US-PAT-NO: 5989963

DOCUMENT-IDENTIFIER: US 5989963 A

TITLE: Method for obtaining a steep retrograde channel profile

--------- KWIC ---------

FIG. 1 is a flow diagram showing selected steps in a prior art manufacturing process to manufacture a semiconductor device. The first step, indicated at 100, is to start with a substrate. A screen oxide layer, also known as a protective oxide layer or a barrier layer, is formed on the substrate in the next step, indicated at 102. One or more ion implant processes are performed on the substrate through the screen oxide layer at the next step, indicated at 104. After the one or more ion implant process, the screen oxide layer is removed, indicated at 106. After the screen oxide layer is removed, a high quality gate oxide is formed on the substrate, indicated at 108. The step, indicated at 110, represents the remaining process steps in the manufacture of the semiconductor device. The remaining steps of the manufacturing process will not be discussed.

FIG. 2A illustrates the process of implanting one or more implants into the

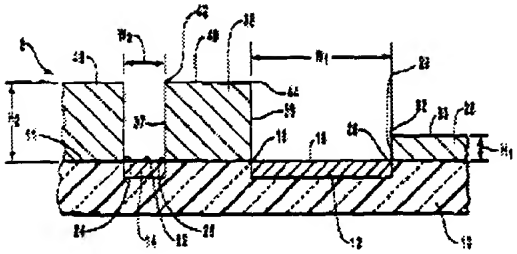


FIG. 1

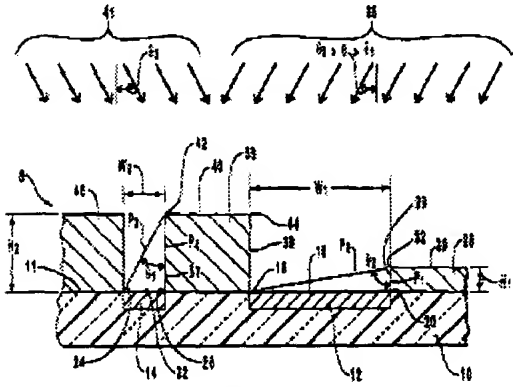


FIG. 2

FIG. 4A

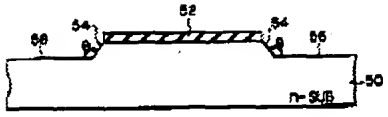


FIG. 4B

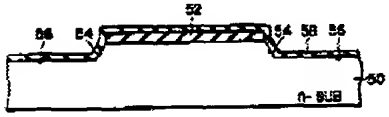
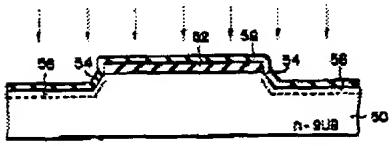
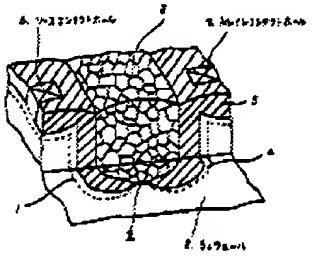
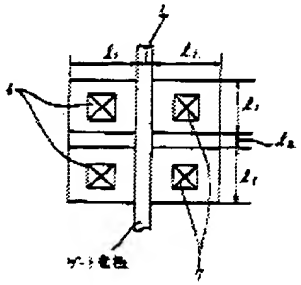


FIG. 4C



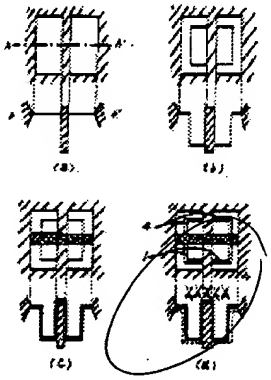


第 1 図

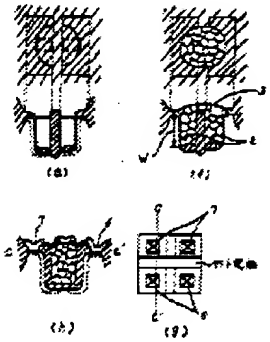


本発明の実施ゲート2 MOSFET

第 2 図



製造工程
第 3 図



製造工程
第 3 図